IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently amended) A processor, comprising:

at least one register file;

at least one execution unit coupled to the at least one register file, the at least one register file being available to programs for temporarily storing operands and results;

at least one bypass circuit operatively coupled to said at least one register file and said at least one execution unit, said at least one bypass circuit capable of arbitrating access by said at least one execution unit to said at least one register file; and

a backing register file comprising a plurality of registers, the backing register file being operatively coupled to said at least one register file, said backing register file being inaccessible to the at least one execution unit and, in at least one mode, is always visible outside the processor and is directly accessible to instructions in ~~available to~~ the programs at any privilege level ~~such that each of the plurality of registers is accessible at random using a uniquely assigned address~~.

2. (Previously presented) The processor of claim 1, wherein the at least one register file comprises a plurality of register files, each execution unit of the at least one execution unit being operably connected to only one register file of said plurality of register files, said backing register file being operably connected to each register file of said plurality of register files thereby allowing a transfer of values from any designated location in any designated register file of said plurality of register files to any designated location in said backing register file, and from any designated location in said backing register file to any designated location in any designated register file of said plurality of register files.

3. (Currently amended) The processor of claim 1, further comprising:

a first connection operably connected to said backing register file from each of the at least one register file, the first connection comprising a full set of address and data lines allowing the backing register file to address and access individual registers and each of the at least one register file; and

a second connection operably connected to a main memory from the said backing register file, the connection circuit providing a series of connections and interfaces placing the backing register file in communication with the main memory.

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20. (Previously presented) The processor of claim 1 wherein the backing register file is further operable in a windowing mode wherein the backing register file mimics register windowing functionality wherein less than all the registers in the backing register file is accessible to a particular process at one time.

21. (Previously presented) The processor of claim 20 wherein the backing register file operates in one of the windowing mode or the native mode depending upon instructions in a current instruction stream of a current process, wherein when the instruction stream includes register windowing instructions, the backing register file operates in the windowing mode, and when the instruction stream does not include register windowing instructions then the backing register file operates in the native mode.

22. (Currently amended) A backing register file for a processor, the backing register file comprising a plurality of registers, the backing register file being operatively coupled to at least one register file, the at least one register file being operatively coupled to at least one execution unit, said backing register file being inaccessible to the at least one execution unit and, in at least one mode, the backing register file is always visible outside the processor and is directly accessible to instructions in ~~available to~~ the programs at any privilege

level ~~such that each of the plurality of registers is accessible at random using a uniquely assigned address~~.

23. (Previously presented) The backing register file of claim 22, wherein the at least one register file comprises a plurality of register files, said backing register file being operably connected to each register file of said plurality of register files thereby allowing a transfer of values from any designated location in any designated register file of said plurality of register files to any designated location in said backing register file, and from any designated location in said backing register file to any designated location in any designated register file of said plurality of register files.

24. (Previously presented) The backing register file of claim 22, wherein the backing register file is further operable in a windowing mode wherein the backing register file mimics register windowing functionality wherein less than all the registers in the backing register file is accessible to a particular process at one time.

25. (Previously presented) The backing register file of claim 24, wherein the backing register file operates in one of the windowing mode or the native mode depending upon instructions in a current instruction stream of a current process, wherein when the instruction stream includes register windowing instructions, the backing register file operates in the windowing mode, and when the instruction stream does not include register windowing instructions then the backing register file operates in the native mode.

26. (New) The processor of claim 1, wherein each of the plurality of registers is accessible at random using a uniquely assigned address.

27. (New) The backing register file of claim 22, wherein each of the plurality of registers is accessible at random using a uniquely assigned address.